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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,310	08/30/2000	Shunpei Yamazaki	07977/151002/US3339D1	2287

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EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,310	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	Kenneth A Parker	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,11,15,19,22-34,36 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,11,15,19,22-34,36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obvious to one of ordinary skill ness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to one of ordinary skill at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims1, 3-5, 8, 10, 15, 22, 24-30, 31-32, are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa 5250931 in view of Lebrun et al 5606194, Adachi et al, 5155612, Kondo 5625473 and Nishiguchi et al 5621553.

Claim 1 is written to A display device comprising: a pair of substrates;an active matrix circuit and peripheral driver circuit provided on one of the pair of the substrates; and a sealing member formed substrates so to seal the peripheral driver circuit, with sealing member being capable light blocking wherein said sealing member comprises a **pigment for light blocking**. Claim 8 is an electronic device comprising: first substrate and a second substrate; a driver circuit region formed on said first substrate, said diver circuit region having at least one of a register circuit, NAND circuit, level shifter circuit and a buffer circuit; an active matrix region formed on said first substrate, said active matrix region having at least a pixel; a sealing member formed between said first and second substrates, said sealing member bonding said first and second substrates and covering said driver circuit region; wherein said sealing member

shields said wherein said sealing member comprises **a pigment for light blocking.** Clam 16 is a display device comprising: at least a first substrate and a second substrate; formed on said first a driver circuit region substrate, said diver circuit region having at least a register circuit, a NAND circuit, a level shifter circuit, **OR** a buffer circuit, wherein at least a CMOS transistor is formed in driver circuit region, CMOS thin film transistor and a first n-channel p-channel thin film transistor; an active matrix region formed said first substrate, said active matrix region having at least a pixel, wherein a second p-channel film transistor formed in said pixel; a sealing member formed between said first and second substrates and covering said driver circuit region; and sealing member bonding said first and second wherein **said sealing member comprises pigment light blocking and wherein said sealing member shields said driver circuit region from light.**

Misawa discloses a liquid crystal device with P and N type cmos transistors in the driver circuits which include a buffer, and P or N drivers in the active region. The device includes the use as a projectior, and is not shown with a black matrix. Lacking is the sealant over the circuit with a pigment for blocking light. Lebrun et al teaches that using a sealant over the circuit (figure 1) enables the low cost protection, and having the sealant be opaque gives the added benefit of protecting the circuit from light. Therefore it would have been obvious to one of ordinary skill , in the device of Misawa, to employ an opaque seal for enclosing the liquid crystal and bonding the substrate to cover the circuit for the low cost protection form the enviroment and light. Still lacking is the use of a pigment.

Adachi et al teaches that the sealants need to be able to block light, and adds pigments to the dyes to assure sufficient light blocking (col. 7, lines 16-20). Therefore it would have been obvious to one of ordinary skill , in the device of Hayashi, to use a light blocking sealant with coloring agents (pigment), to ensure sufficient light blocking as taught by Adachi et al. Many of the low cost conventional sealants, such as polyimide and acrylic require pigment pigments to block light. Therefore, it would have been obvious to one of ordinary skill to employ pigments in order to enable use of the conventional low cost materials.

The rejection can be viewed as Lebrun in view of Misawa and the two secondary references Adachi and Castleberry, both provided to show the well known nature of the use of dyes for creating light blocking sealants. Misawa teaches that their CMOS active matrix and drivers enables low cost with a high reliability and resolution (column 2, lines 38-40). Therefore, it would have been obvious to one of ordinary skill , in the device of Lebrun, to employ the CMOS active matrix and driver structure of Misawa for the benefits of low cost with a high reliability and resolution. This teaching of Misawa was, at the time of invention, notoriously well known, and would have been further obvious to one of ordinary skill for that reason. For this version, still lacking is the use of a pigment. Adachi et al teaches that the sealants need to be able to block light, and adds pigments to the dyes to assure sufficient light blocking (col. 7, lines 16-20). Therefore it would have been obvious to one of ordinary skill , in the device of Hayashi, to use a light blocking sealant with coloring agents (pigment), to ensure sufficient light blocking as taught by Adachi et al.

Sealants were conventionally put on alignment layers, avoiding unnecessary processing to remove them in the areas where the light blocking layers are form. The references to Kondo and Nishiguchi et al evidence this. Therefore it would have been obvious, in the devices of Misawa as modified above (or Lebrun for the reversed situation), to put the sealant above the alignment layers to avoid having to remove them.

Claims 5, 7, 15 and 21 are a display device according to claim 1 wherein the substrates are bonded each other with the sealing member and a device according to claim 1 further comprising a liquid crystal material between the substrates, wherein the sealing member seals the liquid crystal material and claim 15 is a device according claim 8 further comprising liquid crystal material injected between the first and the second substrate. Claim 21 is a device according claim 16 further comprising a liquid crystal material injected between the first substrate and the second substrate. These are met by Misawa as modified by Lebrun as the Misawa is modified to include the light blocking seal of Lebrun which provides these functions. Claims 10 and 18 are a device according to claim 8 wherein said shift register circuit comprises least a clocked inverter and inverter. As the shift register is part of the OR, so is met by the buffer whether or not this claim language is met. Regarding claim 14 which is an electronic device according to claim 8 wherein said device is a projector, the projector is explicitly taught by the Misawa. Claim 3 is a display device according claim 1 wherein one of an electrode or a wiring line connected to a source or drain of a thin-film transistor formed in the matrix circuit is one of a metal film, a

semiconductor film, and a silicide film, and wherein a light blocking film for the thin-film transistor is formed by using the one the of the metal film, the semiconductor film, and a silicide film. This is met by the combined references as the secondary reference places a light blocking film over all of the elements of the driver circuit.

Claim 4 is a display device according to claim 1 wherein said pair of the substrates are glass substrates or quartz substrates. These were the conventionally used materials, and would have been obvious to one of ordinary skill for that reason.

Inverters were conventionally used as a fundamental building block required to build driving circuits, and so to the reason to use them was to use the use the established technology. Therefore it would have been obvious, in the device of the references above, to employ inverters as was conventionally used for the benefit of using the established technology.

Claims 2, 6, 7, 11 and 19, 23, 33-34, 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa 5250931in view in view of Lebrun et al 5606194, Adachi et al, 5155612, Kondo 5625473 and Nishiguchi et al 5621553 as applied above, and further in view of Wakai 5003356.

Claims 2, 9 and 7 are a display device according claim 1 wherein active matrix circuit has pixels arranged in matrix form, and wherein regions in each of the pixels where source lines and drain lines overlap with a pixel electrode form a black matrix. Claim 9 is a device according to claim 8 wherein said device does

not include a black matrix. Claim 17 is a device according to claim 16 wherein said device does not include a black matrix. The use of the pixels overlapping the gate and source lines was a notoriously well known method of providing a low cost black matrix in liquid crystal devices. This is evidenced by Wakai . Therefore it would have been obvious to one of ordinary skill to overlap these for the benefit of the low cost.

Claims 6, 11 and 19 are a device according to claim 1 further comprising: at least CMOS transistor formed in the driver circuit region, said CMOS transistor having an n-channel thin film transistor and a p-channel thin transistor;a film transistor formed in each pixel in the active matrix circuit, said thin film transistor having at an active layer, to said active layer, a gate electrode adjacent to said gate insulating film, wherein light blocking film is formed said gate electrode. Claim 19 is substantially a device according to claim 16 wherein, said first p-channel thin film transistor comprises, first source region and a first drain region formed over said first substrate, a first channel forming region formed between said first region and source regions, a first gate insulating region formed adjacent to said source and drain regions and said first channel forming region, a first gate electrode formed adjacent to said first gate insulating film, said n-channel thin film transistor comprises, a third region and a third drain region formed over said first substrate, a third channel forming region formed between said third source and drain regions, a third gate insulating region formed adjacent to said third source and drain regions and said third channel forming region, a third gate electrode formed adjacent to said third gate insulating film, said second p-

channel thin film transistor comprises, second source region and a second drain region formed over said first substrate, a second channel forming region formed between second source and drain regions, second gate said second source and drain regions and second channel forming region second gate electrode formed adjacent said second gate insulating film, wherein a second gate electrode, with light blocking film is formed. Claim 11 is a device according claim 8 further comprising: at least a CMOS transistor formed in said driver circuit region, said CMOS transistor having an n-channel thin transistor and a p-channel thin transistor; a thin film transistor formed in said pixel, said thin film transistor having at least an active layer, a gate insulating film adjacent said active layer, a gate electrode adjacent to said gate insulating film, and further comprising a light blocking film formed over said gate electrode. It was well known to employ a light block as claimed to prevent light activation. This is evidenced by Wakai, which teaches such a structure for this benefit (figure 13 and related discussion). Therefore would have been obvious to one of ordinary skill to use a metal light block near the gate for the reasons taught by Wakai and well known in the art.

Sealants were conventionally put on alignment layers, avoiding unnecessary processing to remove them in the areas where the light blocking layers are form. The references to Kondo and Nishiguchi et al evidence this. Therefore it would have been obvious, in the devices of Misawa as modified above (or Lebrun for the reversed situation), to put the sealant above the alignment layers to avoid having to remove them.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth A Parker
Primary Examiner
Art Unit 2871